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| Course Title | Microprocessor Systems and Interfacing | | | | | Course Code | EEE342 | | Credit Hours | 4 |
| Instructor | Engr. Usman Rafique | | | | Program | BSTE | | | | |
| Semester: | 6th | Batch | FA12 | Section | A | Date | | March 13, 2015 | | |
| **Submission Date:** | **March 20, 2015 (During class time)** | | | | | **Marks:** | | **40** | | |
| **Assignment 1** | | | | | | | | | | |
| **Instructions:**   * Follow the guidelines for assignment submission as given in course hand book. * Add front title to the solution as described in the class room. * No solution shall be accepted after due date and time. | | | | | | | | | | |

Question 1 20 Marks

Interface 256KB SRAM with 8088 CPU. Design your memory system using four 16KB SRAM chips, two 32KB SRAM chips and one 128KB SRAM chip. Memory map for total SRAM starts from C0000H and above. You are required to provide:

1. Completely labelled schematic diagram of interfacing SRAM and CPU 12 Marks
2. Memory map for each SRAM chip 8 Marks

Question 2 10 Marks

Consider you have to add the contents of two data memory segments named as SEG\_A and SEG\_B. The sum is to be stored in a third data segment called SEG\_RES. Example of the required operation is given in figure below for byte 0. You are required to write an assembly language program that performs this operation on all bytes in SEG\_A and SEG\_B.

Segment addresses for SEG\_A, SEG\_B and SEG\_RES are 1000H, 2000H and C000H, respectively.



Figure 1

Question 3 10 Marks

Interface 128 KB EEPROM with 8088 CPU. Your design must use 32KB EEPROM chips only. Only decoder that you may use in your design is 74LS138. Memory map for total ROM starts from E0000H and above. Provide:

1. Completely labelled schematic diagram of interfacing EEPROM with CPU 6 Marks
2. Memory map for each EEPROM 4 Marks